IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate having an uppermost insulating film;

lamination of a first conductive film of metal or metal silicide, a first insulating film, and a second insulating film made of silicon nitride laminated in this order from a lower side, the lamination being formed on or above the uppermost insulating film, and having a same pattern defined with a pair of side walls;

a pair of third insulating films formed on the pair of side walls of the lamination covering at least the first conductive film, the third insulating film being made of a same material as the first insulating film, and having a thickness smaller than that of the first insulating film;

a pair of fourth insulating films formed on the pair of side walls of the lamination through said third insulating films, to be contiguous to said second insulating film, the second and the fourth insulating films collectively covering the first conductive film;

an interlevel insulating layer formed on or above said semiconductor substrate, covering said second and fourth insulating films;

an aperture formed through said interlevel insulating layer, at least partially exposing one of said fourth insulating films; and

a second conductive film filling the aperture.

Claim 2 (Previously Amended): A semiconductor device according to claim 1, wherein said first insulating film and said pair of third insulating films cover the side wall and upper surface of said first conductive film.

Claim 3 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate having an uppermost insulating film;

lamination of a first conductive film made of metal or metal silicide, a first insulating film, and a second insulating film made of silicon nitride laminated in this order from a lower side, the lamination being formed on or above the uppermost insulating film, and having a same pattern defined with a pair of side walls;

a pair of third insulating films formed on the pair of side walls of the lamination covering at least the first conductive film, the third insulating film having a thickness smaller than that of the first insulating film, the first and third insulating films being made of different materials except silicon nitride;

a pair of fourth insulating films formed on the pair of side walls of the lamination through said third insulating films, to be contiguous to said second insulating film, the second and the fourth insulating films collectively covering the first conductive film;

an interlevel insulating layer formed on or above said semiconductor substrate, covering said second and fourth insulating films;

an aperture formed through said interlevel insulating layer, at least partially exposing one of said fourth insulating films; and

a second conductive film filling the aperture.

Claim 4 (Previous Amended): A semiconductor device according to claim 1, wherein said third insulating film extends under a bottom end of said fourth insulating film positioned on the side wall of said first conductive film.

Claim 5 (Previously Amended): A semiconductor device according to claim 1, wherein said first conductive film is a gate electrode of a MIS transistor.

Claim 6 (Previously Amended): A semiconductor device according to claim 1, wherein said third insulating film is made of a silicon oxide film.

Claim 7 (Original): A semiconductor device according to claim 2, wherein said first insulating film is thicker at the upper surface of said conductive pattern than at the side wall thereof.

Claim 8 (Previously Amended): A semiconductor device according to claim 1, wherein said interlevel insulating film has etching characteristics different from a silicon nitride film and is formed on said second insulating film made of a silicon nitride.

Claim 9 (Previous Amended): A semiconductor device according to claim 8, wherein the surface of said interlevel insulating layer is generally parallel to said semiconductor substrate.

Claim 10 (Canceled)

Claim 11 (Previously Amended): A semiconductor device according to claim 8, further comprising:

a fifth insulating film formed on the interlevel insulation layer and defining a contact area on said second conductive film.

Claim 12 (Previously Amended): A semiconductor device according to claim 11, further comprising:

an upper conductive pattern formed on said fifth insulating film and on said second conductive film;

a sixth insulating film made of an insulating material other than silicon nitride, and formed to cover at least a side wall of said upper conductive pattern; and

a seventh insulating film made of silicon nitride and formed to continuously cover said upper conductive pattern and said sixth insulating film.

Claim 13 (Previously Amended): A semiconductor device according to claim 12, further comprising:

another contact area formed in said interlevel insulating layer on an opposite side of said first conductive film to said contact area, having a bottom portion at least partially defined by said fourth insulating film; and

another conductive film filling said another contact area;

wherein said fifth insulating film further defines another contact area on said another conductive g film.

14. (Previously Amended): A semiconductor device according to claim 13, further comprising a storage capacitor formed on said another conductive film.

Claim 15 (Previously Amended): A semiconductor device according to claim 14, wherein said storage capacitor is formed to at least partially cover said seventh insulating film.

Claim 16 (Previously Amended): A semiconductor device according to claim 12, further comprising:

an eighth insulating film made of silicon nitride formed between said interlevel insulating film and fifth insulating film, and cooperatively defining said contact area with said interlevel insulating layer.

Claim 17 (Previously Amended): A semiconductor device according to claim 14 , further comprising:

a field insulating film formed on a surface of said semiconductor substrate, and having a surface at a higher level than said insulating surface of said substrate;

wiring patterns formed on said field insulating film and on said fifth insulating film; and

silicon nitride layers covering said wiring patterns.

Claim 18 (Previously Amended): A semiconductor device according to claim 17, further comprising:

an interlayer insulating layer covering said fifth insulating layer, said storage capacitor, and said silicon nitride layer covering the wiring pattern on said fifth insulating film;

connection holes formed through said interlayer insulating layer and reaching said wiring patterns; and

upper wiring patterns.

Claim 19 (Previously Amended): A semiconductor device according to claim 18, wherein said storage capacitor includes a storage electrode connected to said another conductive film, a dielectric film formed on said storage electrode and on said fifth insulating film, and an opposing electrode formed on said dielectric film and having an extension on said fifth insulating film, one of said connection holes penetrates through said opposing electrode at said extension, and one of said upper wiring patterns makes electrical contact with said opposing electrode at its side wall.

Claims 20-61 (Canceled)

Claim 62 (Previously Amended): A semiconductor device according to claim 3, wherein said third insulating film extends under a bottom end of said fourth insulating film positioned on the side

wall of said lamination.

Claim 63 (Previously Amended): A semiconductor device according to claim 3, wherein said first conductive film is a gate electrode of a MIS transistor.

Claim 64 (Previously Amended): A semiconductor device according to claim 3, wherein said third insulating film is made of a silicon oxide film.

Claim 65 (Previously Amended: A semiconductor device according to claim 3, wherein said interlevel insulating layer has etching characteristics different from a silicon nitride film and is formed on said second insulating film made of a silicon nitride.

Claim 66 (Previously Amended): A semiconductor device according to claim 1, wherein said first conductive film forms a bit line of a dynamic random access memory.

Claim 67 (Previously Amended): A semiconductor device according to claim 3, wherein said first conductive film forms a bit line of a dynamic random access memory.

Claim 68 (Previously Added): A semiconductor device according to claim 3, wherein the first insulating film is made of silicon oxy-nitride.

Claim 69 (Previously Added): A semiconductor device according to claim 3, wherein the surface of said interlevel insulating layer is generally parallel to said semiconductor substrate.

Claim 70 (Canceled)

Claim 71 (Previously Amended): A semiconductor device according to claim 65, further comprising:

a fifth insulating film formed on the interlevel insulation layer and defining a contact area on said second conductive film.

Claim 72 (Previously Amended): A semiconductor device according to claim 71, further comprising:

an upper conductive pattern formed on said fifth insulating film and on said second conductive film;

a sixth insulating film made of an insulating material other than silicon nitride, and formed to cover at least a side wall of said upper conductive pattern; and

a seventh insulating film made of silicon nitride and formed to continuously cover said upper conductive pattern and said sixth insulating film

Claim 73 (Previously Amended): A semiconductor device according to claim 72, further comprising:

another contact area formed in said interlevel insulating layer on an opposite side of said first conductive film to said contact area, having a bottom portion at least partially defined by said fourth insulating film; and

another conductive film filling said another contact area;

wherein said fifth insulating film further defines another contact area on said another conductive film.

Claim 74 (Previously Amended): A semiconductor device according to claim 73, further comprising a storage capacitor formed on said another conductive film.

Claim 75 (Previously Added): A semiconductor device according to claim 74, wherein said storage capacitor is formed to at least partially cover said seventh insulating film.

Claim 76 (Previously Added): A semiconductor according to claim 75, further comprising:

an eighth insulating film made of silicon nitride, formed between said fourth and fifth insulating films, and cooperatively defining said contact area with said fourth insulating film.

Claim 77 (Previously Added): A semiconductor device according to claim 76, further comprising:

a field insulating film formed on a surface of said semiconductor substrate, and having a surface at a higher level than said insulating surface of said substrate;

wiring patterns formed on said field insulating film and on said fifth insulating film; and

silicon nitride layers covering said wiring patterns.

Claim 78 (Previously Added): A semiconductor device according to claim 77, further comprising:

an interlayer insulating layer covering said fifth insulating layer, said storage capacitor, and said silicon nitride layer covering the wiring pattern on said fifth insulating film;

connection holes formed through said interlayer insulating layer and reaching said wiring patterns; and

upper wiring patterns.

Claim 79 (Previously Amended): A semiconductor device according to claim 78, wherein said storage capacitor includes a storage electrode connected to said another conductive film, a dielectric film formed on said storage electrode and on said fifth insulating film, and an opposing electrode formed on said dielectric film having an extension on said fifth insulating film one of said connection holes penetrates through said opposing electrode at said extension, and one of said upper wiring patterns makes electrical contact with said opposing electrode at its side wall.